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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,224	11/19/2001	Christopher K. Sutton	10990531-1	5410

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EXAMINER

LAU, TUNG S

ART UNIT PAPER NUMBER

2863

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/992,224

Applicant(s)

SUTTON ET AL.

Examiner

Tung S Lau

Art Unit

2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8-11, 14, 16, 18, 21, 23 is/are rejected.
- 7) ☒ Claim(s) 6, 7, 12, 13, 15, 17, 19, 20, 22 and 24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3-15-04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 11, 21, 23, 2, 4, 5, 8, 9, 10, 14, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Momohara (U.S. Patent 6,094,733).

Regarding claim 1:

Momohara discloses an electronic test system for testing an electronic device under test (DUT), said test system comprising an electronic processor (Col. 4-5, Lines 20-15); an electronic memory coupled to said electronic processor (fig. 8, unit 102, 9); a hierarchical program structure residing in said memory and executed by said processor (fig. 14-24b), said hierarchical program structure having multiple levels including a measurement level corresponding to a measurement to be performed on said DUT (fig. 14-24b), to a test level corresponding to one or more of said measurements (fig. 9), and a procedure level corresponding to an ordered list of said tests to be performed on said DUT (fig. 8, unit 150).

Regarding claim 3:

Momohara discloses an electronic test system for testing an electronic device under test (DUT), said test system comprising an electronic processor (fig. 8, unit 102); an electronic memory coupled to said electronic processor (fig. 8, unit 103); a hierarchical program structure residing in said memory and executed by said processor (fig. 14-24b), said hierarchical program structure having multiple levels including a measurement level corresponding to a measurement to be performed on said DUT (fig. 9), a test level corresponding to one or more of said measurements (fig. 9), and a procedure level corresponding to an ordered list of said tests to be performed on said DUT (fig. 11), each said level embodied in said electronic test system as a software object (Col. 4-5, Lines 20-15).

Regarding claim 11:

Momohara discloses an electronic test system comprising an electronic processor (fig. 8, unit 102); an electronic memory coupled to said electronic processor (fig. 8, unit 103); a hierarchical structure residing in the memory and executed by said processor (Col. 4-5, Lines 20-15), said hierarchical structure having multiple levels (fig. 9), each level embodied in the electronic test system as a function defined by a class (Col. 4-5, Lines 20-15), wherein the implementation of the function is defined by the user of the hierarchical structure by implementing the class (Col. 4-5, Lines 20-15, fig. 9); said classes including a measurement class corresponding to a measurement to be performed on said device (fig. 9), a test class corresponding to one or more related measurements

(Col. 4-5, Lines 20-15), and a procedure class corresponding to an ordered list of tests to be performed on said device (fig. 21a).

Regarding claim 21:

Momohara discloses a method for producing an electronic test system software program for testing an electronic device under test (DUT), said program including a hierarchical structure having multiple levels including a measurement level corresponding to a measurement to be performed on said DUT (Col. 4-5, Lines 20-15, fig. 9), a test level corresponding to one or more of said measurements (fig. 9), and a procedure level corresponding to an ordered list of said tests to be performed on said DUT (Col. 4-5, Lines 20-15, fig. 9), each level embodied in said program as a software object for testing a device under test (DUT) (fig. 8, unit 150), said method comprising the steps of providing a set of functions wherein the implementation of the functions is defined by said hierarchical structure (Col. 4-5, Lines 20-15, fig. 9); implementing the functions to define said test system software program (Col. 4-5, Lines 20-15, fig. 9, 15); generating said electronic test system software objects by implementing said functions (fig. 15); and utilizing said software objects to test said DUT (fig. 15).

Regarding claim 23:

Momohara discloses a computer-readable medium on which is stored a program for testing an electronic device under test (DUT) (fig. 8, unit 150), said computer program comprising a measurement software object corresponding to a measurement to be performed on said DUT (fig. 9); a test software object defining a test algorithm utilizing parameters provided by said measurement object and corresponding to a test to be performed on said DUT (Col. 4-5, Lines 20-15); a procedure software object corresponding to an ordered list of said tests to be performed on said DUT (fig. 16); and a plurality of software pointers linking said measurement object, said test object (fig. 9), and said procedure object (fig. 13).

Regarding claim 2, 4, 5, 8, 9, 10, 14, 16 and 18:

Momohara also disclose an electronic test system wherein said hierarchical program structure further includes a datapoint level corresponding to a single result of a measurement, and said measurement level includes a plurality of said datapoints (fig. 9); an electronic test system wherein said hierarchical program structure further includes a datapoint level, and said measurement level corresponds to a group of said datapoints, said datapoint level embodied in said electronic test system as a datapoint software object (fig. 9); An electronic test system wherein said hierarchical program structure further includes a product

model level corresponding to a set of procedures for testing a family of said DUT (fig. 8); An electronic test system wherein said test object defines a test-algorithm (fig. 16). An electronic test system wherein said test algorithm comprises one or more electronic operations defined by software code, and the electronic parameters for said electronic functions are provided by said measurement lo object (15-24a). An electronic system wherein said test object contains said measurement object, and said measurement object contains said datapoint object (fig. 9). An electronic test system wherein said electronic processor further is adapted for electronically communicating with said DUT for executing said test software on said DUT and receiving a plurality of electronic outputs from said DUT corresponding to said measurement objects and said datapoint objects (fig. 9). An electronic test system comprising plug-in software code components residing in said memory and providing an interface to other systems (Col. 4-5, Lines 20-15, fig. 14). Software object ending and beginning test (fig. 15-21b).

Claim Objections

2. Claims 6, 7, 12, 13, 15, 17, 19, 20, 22, 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to teach use of dll file; the object component modal as CPM objects, the class linked to measurement class, capable of beginning and ending the selected process, controlling temperature and humidity, use of a touch pad, Active X Com interface, data point which linked to measurement objects, a second set of object methods for creating a test and procedure object containing test object. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments filed 3/8/2004 have been fully considered but they are not persuasive.

A. Applicant argues in the lengthy arguments that the prior art does not show the 'hierarchical program structure including a measurement level, a test

level and a procedure level. Momohara discloses 'hierarchical program structure including a measurement level, a test level and a procedure level' in abstract and Col. 2, Lines 12-21, fig. 14-24b. the applicant argue that 'hierarchical program' is not a parallel process as Momohara discloses. Remind to the applicant that during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Since the applicant did not define 'hierarchical program' in the specification, according to PTO practice the ordinary term of 'hierarchical program' is use, and the regular meaning of 'hierarchical; means 'related to' according to Merriam Webster online dictionary. Since Momohara talk about his testing all related to DC characteristic (abstract), therefore Momohara testing program is 'hierarchical' as the claimed invention.

B. Applicant continue to argue in the lengthy arguments that the prior art does not show the 'datapoint level testing including plurality of data point'. Momohara discloses 'datapoint level testing including plurality of data point' in fig. 21a, unit st5-st8.

C. Applicant continue to argue in the lengthy arguments that the prior art does not show the 'measurement level test level and procedure level'. Momohara discloses 'measurement level test level and procedure level' in Col. 2, Lines 12-21, fig. 21a16-21.

D. Applicant continue to argue in the lengthy arguments that the prior art does not show the 'multiple level test structure with function define by class'. Momohara discloses 'multiple level test structure with function define by class' in fig. 16-21.

E. Applicant continue to argue in the lengthy arguments that the prior art does not show the 'test algorithm defining test object'. Momohara discloses 'test algorithm defining test object' in fig. 17, unit ST4, fig. 18, unit 108, fig. 21a, unit ST5-ST8.


Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 703-305-3309. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956. TC2800 RightFAX Telephone Numbers : TC2800 Official Before-Final RightFAX - (703) 872-9318, TC2800 Official After-Final RightFAX - (703) 872-9319 TC2800 Customer Service RightFAX - (703) 872-9317

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